SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-045976, filed March 09, 2015; the entire contents of which are incorporated herein by reference.

FIELD

An embodiment described herein relates to a semiconductor device, and particularly, to a semiconductor device that uses a compound semiconductor.

BACKGROUND

An electronic device that uses a nitride semiconductor is used for a high-speed electronic device or a power device. In addition, a light emitting diode (LED) that is a semiconductor light emitting element which uses a nitride semiconductor is used for a display device, illumination, or the like.

A power device requires a high breakdown voltage and a low on-resistance. There is a trade-off relationship that is determined by an element material between a breakdown voltage and an on-resistance, but a wide band gap semiconductor, such as a nitride semiconductor or silicon carbide (SiC) is used as an element material, and thus a trade-off relationship that is determined by a material can be improved, compared to silicon, and a high breakdown voltage and a low on-resistance can be realized. In addition, an element that uses a nitride semiconductor, such as GaN or AlGaN has excellent material properties, and thereby a high-performance power device can be realized.

An example of related art includes JP-A-2013-8836

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a sectional diagram of a semiconductor device according to an embodiment.

FIG. 2 is a diagram illustrating conditions of a gate electrode and a channel layer according to the embodiment.

FIG. 3 is a graph representing a relationship between a gate voltage and a drain current, when a gate length is used as a parameter.

DETAILED DESCRIPTION

[0005]

An embodiment provides a semiconductor device that can reduce current collapse and a leakage current.

[0008]

Hereinafter, an embodiment will be described with reference to the drawings. However, the drawings are schematic and conceptual, and dimensions, proportions, or the like of the respective drawings are not necessarily limited to the same ones as the actual ones. The embodiment described below exemplifies a device and a method in which a technical idea of the invention is embodied, and the technical idea of the invention is not limited by shapes, structures, and arrangement of configuration components, or the like. In the following description, the same symbols or reference numerals will be attached to the elements having the same functions and configurations, and repeated description will be made only when necessary.

1. Structure of Semiconductor Device

[0009]

FIG. 1 is a sectional diagram of a semiconductor device 1 according to an embodiment. The semiconductor device 1 according to the present embodiment is configured by a heterojunction field effect transistor (HFET) or a high electron mobility transistor (HEMT).

The semiconductor device 1 includes a buffer layer 11, a high resistance layer 12, a channel layer 13, a barrier layer 14, and various electrodes that are sequentially laminated on a substrate 10.

[0010]

The substrate 10 is configured by a silicon (Si) substrate in which for example, a (111) plane is used as a main plane. Sapphire (Al2O3), silicon carbon (SiC), gallium phosphide (GaP), indium phosphide (InP), gallium arsenide (GaAs), or the like may be used for the substrate 10. In addition, a substrate including an insulation layer can also be used for the substrate 10. For example, a silicon on insulation (SOI) substrate can be used for the substrate 10. The substrate 10 may be a single crystal substrate on which an epitaxial layer can be grown, and is not limited to those listed above.

[0011]

The buffer layer 11 mitigates distortion caused by a difference between a lattice constant of a nitride semiconductor layer that is formed on the buffer layer 11 and a lattice constant of the substrate 10, and has a function of controlling crystalline of the nitride semiconductor layer that is formed on the buffer layer 11. In addition, the buffer layer 11 has a function of suppressing a chemical reaction between an element (for example, gallium (Ga)) that is contained in the nitride semiconductor layer which is formed on the buffer layer 11 and an element (for example, silicon (Si)) of the substrate 10. The buffer layer 11 is configured by, for example, AlXGa1-XN (0£X£1). In the present embodiment, the buffer layer 11 is configured by AlN. The buffer layer 11 is not an essential element of the present embodiment, and may be omitted.

[0012]

The high resistance layer 12 has a function of increasing a breakdown voltage of the semiconductor device 1, and mainly increases a breakdown voltage between a drain electrode and the substrate. That is, by providing the high resistance layer 12, a voltage according to a resistance of the high resistance layer 12 is applied to the high resistance layer 12, and thereby the breakdown voltage can be increased by the amount of the voltage. The high resistance layer 12 is configured by a nitride semiconductor layer in which carbon (C) is doped, and the nitride semiconductor layer is configured by, for example, InXAlYGa(1-X-Y)N (0£X<1, 0£Y<1, 0£X+Y<1). In the present embodiment, the high resistance layer 12 is configured by GaN (C-GaN) in which carbon is doped. A carbon concentration of the high resistance layer 12 is greater than a carbon concentration of the channel layer 13 which will be described below. The carbon concentration of the high resistance layer 12 is set to, for example, 1´1017 cm-3 or more. A resistance value of the high resistance layer 12 is appropriately set in accordance with a breakdown voltage that is desired for the semiconductor device 1. The high resistance layer 12 is not an essential element of the present embodiment, and may be omitted.

[0013]

The channel layer 13 is a layer in which a channel (current path) of a transistor is formed. The channel layer 13 is configured by InXAlYGa(1-X-Y)N (0£X<1, 0£Y<1, 0£X+Y<1). It is preferable that the channel 13 is configured by a nitride semiconductor layer with a good crystalline (high quality). In the present embodiment, the channel 13 is configured by GaN. A more specific configuration of the channel layer 13 will be described below.

[0014]

The barrier layer 14 configures a heterojunction with the channel layer 13. The barrier layer 14 is configured by a nitride semiconductor layer having a greater band gap than that of the channel layer 13. The barrier layer 14 is configured by InXAlYGa(1-X-Y)N (0£X<1, 0£Y<1, 0£X+Y<1). In the present embodiment, the barrier layer 14 is configured by undoped AlGan. The “undoped” means that impurities are not intentionally doped, and for example, an amount of impurities that are injected in a manufacturing process or the like is included in the “undoped”.

[0015]

In the heterojunction of the channel layer 13 and the barrier layer 14, the barrier layer 14 is smaller in lattice constant than the channel layer 13, and thereby distortion occurs in the barrier layer 14. Piezo polarization occurs in the barrier layer 14 by a piezo effect due to the distortion, and two-dimensional electron gas (2DEG) is generated near an interface between the channel layer 13 and the barrier layer 14. The two-dimensional electron gas becomes a channel between a source electrode 15 and a drain electrode 16.

[0016]

A plurality of semiconductor layers that configure the semiconductor device 1 are sequentially formed using, for example, an epitaxial growth that uses a metal organic chemical vapor deposition (MOCVD) method. That is, the plurality of semiconductor layers that configure the semiconductor device 1 is configured by epitaxial layers.

[0017]

The source electrode 15 and the drain electrode 16 are provided on the barrier layer 14 so as to be separated from each other. The source electrode 15 and the 2DEG are in ohmic contact with each other via the barrier layer 14. In the same manner, the drain electrode 16 and the 2DEG are in ohmic contact with each other via the barrier layer 14. That is, both the source electrode 15 and the drain electrode 16 are configured to include materials in ohmic contact with the 2DEG. Titan (Ti), a stacked structure of Al/Ti, or the like is used for the source electrode 15 and the drain electrode 16. The right side of “/” denotes a lower layer, and the left side of “/” denotes an upper layer.

[0018]

A gate electrode 17 is provided on the barrier layer 14 and between the source electrode 15 and the drain electrode 16. In order to increase a breakdown voltage between a gate and a drain, a distance between the gate electrode 17 and the drain electrode 16 is set so as to be longer than a distance between the gate electrode 17 and the source electrode 15. The gate electrode 17 and the barrier layer 14 are in a Schottky junction with each other. That is, the gate electrode 17 is configured to include a material that is in a Schottky junction with the barrier layer 14. The semiconductor device 1 illustrated in FIG. 1 is a Schottky barrier type HEMT. Nickel (Ni), a stacked structure of Au/Ni, or the like is used for the gate electrode 17.

[0019]

A drain current can be controlled by a Schottky barrier that is generated by a junction of the gate electrode 17 and the barrier layer 14. In addition, mobility of carriers that flow in the two-dimensional electron gas is fast, and thereby the semiconductor device 1 can perform a very fast switching operation.

[0020]

The semiconductor device 1 is not limited to a Schottky barrier type HEMT, and may a metal insulator semiconductor (MIS) type HEMT in which a gate insulating film is interposed between the barrier layer 14 and the gate electrode 17. In addition, a junction type gate structure may be applied to the HEMT. The junction type gate structure is configured in such a manner that a p type nitride semiconductor layer (for example, GaN layer) is provided on the barrier layer 14, and the gate electrode 17 is provided on the p type nitride semiconductor layer.

1. Configuration of Field Plate Electrode

[0021]

The semiconductor device 1 includes a field plate electrode (gate field plate electrode) that is electrically coupled to the gate electrode 17, and a field plate electrode (source field plate electrode) that is electrically coupled to the source electrode 15. That is, the semiconductor device 1 includes a so-called double field plate structure.

[0022]

An interlayer insulating layer 20 is provided on the gate electrode 17 and the barrier layer 14. Silicon oxide (SiO2), silicon nitride (SiN), a high dielectric (high-k) material, or the like is used for the interlayer insulating layer 20. Hafnium oxide (HfO2) or the like is used for the high-k material.

[0023]

A gate field plate electrode 21 is provided on the interlayer insulating layer 20. The gate field plate electrode 21 is electrically coupled to the gate electrode 17 via a contact 22. The gate field plate electrode 21 extends toward the drain electrode 16 from top of the gate electrode 17. An end of the gate field plate electrode 21 is disposed on the drain electrode 16 side, rather than an end of the gate electrode 17.

[0024]

An interlayer insulating layer 23 is provided on the gate field plate electrode 21 and the interlayer insulating layer 20. Silicon oxide (SiO2), silicon nitride (SiN), a high-k material, or the like is used for the interlayer insulating layer 23.

[0025]

A source field plate electrode 24 is provided on the interlayer insulating layer 23. The source field plate electrode 24 is electrically coupled to the source electrode 15 via a contact 25. The source field plate electrode 24 extends toward the drain electrode 16 from top of the source electrode 15. An end of the source field plate electrode 24 is disposed on the drain electrode 16 side, rather than an end of the gate field plate electrode 21.

[0026]

An electrode 26 is provided on the drain electrode 16. A protection layer 27 is provided on the source field plate electrode 24 and the electrode 26. The protection layer 27 is also referred to as a passivation layer. The protection layer 27 is configured by an insulating layer, and silicon nitride (SiN), silicon oxide (SiO2), or the like is used for the protection layer 27.

[0027]

A field plate electrode is not an essential requirement of the present embodiment, and thus, the semiconductor device 1 may not include a field plate electrode. In addition, the semiconductor device 1 may include only one of the gate field plate electrode and the source field plate electrode.

2. Relationship between Gate Electrode 17 and Channel Layer 13

[0028]

In an HEMT (also referred to as HFET) that is used as the semiconductor device 1, there is a case in which a leakage current at the time of OFF is increased by threshold voltage variation due to, for example, drain induced barrier lowering (DIBL). In addition, if a gate length is shortened in order to increase operation speed, the influence of a short channel effect (SCE) is increased, and a leakage current that is generated by punch-through increases. The short channel effect is a phenomenon in which, if a gate length of a transistor is shortened, it is difficult for the control of carriers according to a gate voltage to be effectively performed. Even when an OFF voltage is applied to a gate of a transistor, a drain current (leakage current) easily flows by the short channel effect. A gate length (there is also a case in which the gate length is referred to as a channel length) is a length of a gate electrode in a direction between a source electrode and a drain electrode.

[0029]

By doping carbon (C) into a GaN layer that is used as the channel layer 13, the short channel effect can be reduced, and when a transistor is OFF, the control of a drain current that is generated by a gate voltage can be improved. However, current collapse is increased, and in addition, mobility is decreased due to impurities (for example, carbon). The current collapse is a phenomenon in which an ON resistance of a transistor in a high voltage operation is increased, in proportion to an ON resistance of a transistor in a low voltage operation. If mobility is decreased, a resistance value of a channel (2DEG) is increased, and an ON resistance (Ron) is increased.

[0030]

Accordingly, in the present embodiment, the thickness of the channel layer 13 is greater and thereby current collapse is reduced, and a gate length is longer and thereby a short channel effect is reduced. FIG. 2 is diagram illustrating conditions of the gate electrode 17 and the channel layer 13 according to the present embodiment.

[0031]

In the present embodiment, if a length of the gate electrode 17 is referred to as Lg and a thickness of the channel layer 13 that is configured by a GaN layer is referred to as Tch, a relationship thereof is represented by the following Expression (1).

Lg>2´Tch ×××(1)

In addition, if the gate length Lg is lengthened, OFF characteristic is improved, but a travel distance of an electron is lengthened, and thereby, an ON resistance is increased, and as a result, operation speed is decreased. From this viewpoint, in the present embodiment, it is preferable that the gate length Lg is equal to or smaller than five times the thickness Tch of the channel layer 13. In addition, it is preferable that, in order to further increase the operation speed, the gate length Lg is equal to or smaller than three times the thickness Tch of the channel layer 13.

[0032]

In addition, the channel layer 13 includes carbon (that is, carbon is doped into the channel layer 13), and a carbon concentration of the channel layer 13 is set to a value less than 1´1017 cm-3. By doing this, a decrease of mobility is suppressed and a short channel effect is reduced.

[0033]

The gate length Lg is set in a sequence of the following i and ii.

i. The thickness Tch of the channel layer 13 and the carbon concentration of the channel layer 13 are determined in such a manner that the desired operation characteristics of the semiconductor device 1 can be realized and the current collapse can be reduced.

ii. The gate length Lg is determined using the thickness Tch of the channel layer 13 that is obtained from the section i, and the above Expression (1).

[0034]

FIG. 3 is a graph representing a relationship between a gate voltage and a drain current, when a gate length is used as a parameter. A horizontal axis of FIG. 3 denotes a gate voltage Vg (V) that is applied to a gate electrode, and a vertical axis of FIG. 3 denotes a drain current Id (A). In the graph of FIG. 3, the thickness of a channel layer is set to approximately 1.2 mm. FIG. 3 illustrates a graph at the time of the gate length Lg being changed to three values (Lg=1.3mm, 3.0 mm, 5.0 mm).

[0035]

As can be seen from FIG.3, if the gate length Lg equals 1.3 mm, a leakage current is generated by a short channel effect. In contrast to this, if the gate length Lg equals 3.0 mm, the control of the drain current at the time of a transistor being off can be easily performed, and the leakage current can be reduced. In the same manner, even if the gate length Lg equals 5.0 mm, the same effect as in the case in which the gate length Lg equals 3.0 mm is obtained.

[0036]

In FIG. 3, if the thickness Tch of the channel layer 13 equals 1.2 mm and the gate length Lg equals 3.0 mm, the above Expression (1) is satisfied. In the same manner, if the thickness Tch of the channel layer 13 equals 1.2 mm and the gate length Lg equals 5.0 mm, the above Expression (1) is satisfied.

3. Effects

[0037]

As described above, the present embodiment includes the channel layer 13 that is provided on the substrate 10, the barrier layer 14 that is provided on the channel layer 13 and configures a heterojunction with the channel layer 13, and the gate electrode 17 that is provided on the barrier layer 14. The channel layer 13 and the barrier layer 14 are configured by a compound semiconductor layer, for example, a nitride semiconductor layer. Specifically, the channel layer 13 is configured by a GaN layer, and the barrier layer 14 is configured by an AlGaN layer. In addition, in the present embodiment, trade-off of current collapse and a short channel effect is improved by two technologies, such as (1) carbon is doped into the channel layer 13 within a range in which a current collapse is not affected, and (2) a gate length is extended to a required minimum limit. For this purpose, the gate length Lg of the gate electrode 17 is set to a value greater than twice the thickness of the channel layer 13, and to a value equal to or smaller than five times the thickness of the channel layer 13. In addition, the channel layer 13 contains carbon, and the concentration of the carbon is set to a value lower than 1´1017 cm-3.

[0038]

Thus, according to the present embodiment, a short channel effect can be reduced, and thereby OFF characteristic can be improved, and a leakage current can be reduced. In addition, by containing carbon with a lower concentration than 1´1017 cm-3 in the channel layer 13, it is possible to further reduce a short channel effect. Thus, a gate length can be shortened to a required minimum limit, and thereby it is possible to increase operation speed (mobility). In addition, current collapse can be reduced, and thereby it is possible to increase the operation speed.

[0039]

In addition, if the semiconductor device 1 includes a field plate electrode, a parasitic capacitor that is generated according to the size of a gate electrode is smaller in ratio than a parasitic capacitor of the field plate electrode. For this reason, even if a gate length of a gate electrode is long to a certain extent, a parasitic capacitor that is included in the semiconductor device 1 is not substantially affected.

[0040]

The present embodiment configures a semiconductor device using a nitride semiconductor. However, the present embodiment is not limited to this, and can also apply a compound semiconductor other than a nitride semiconductor.

[0041]

In the present specification, it is assumed that the “nitride semiconductor” includes a semiconductor of all kinds of composition in which composition ratios x and y are changed within a range of each of x and y, in a chemical formula that is InxAlyGa(1-x-y)N (0£x£1, 0£y£1, 0£x+y£1). In addition, it is assumed that, in the above chemical formula, a semiconductor which also further contains V-group elements other than N (nitride), a semiconductor which further contains various types of elements to be contained to control various types of properties such as a conduction type, and a semiconductor which further contains various types elements to be unintentionally contained are contained in the “compound semiconductor”.

[0042]

In the present specification, “lamination” includes a case in which layers overlap each other with a certain layer interposed therebetween, in addition to a case in which the layers overlap in contact with each other. In addition, “provided on something” includes a case in which a certain layer is provided and interposed between layers, in addition to a case in which the layer is provided in direct contact with the layers.

[0043]

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first compound semiconductor layer that is provided on a substrate;

a second compound semiconductor layer that is provided on the first compound semiconductor layer and has a greater band gap than that of the first compound semiconductor layer; and

a gate electrode that is provided on the second compound semiconductor layer,

wherein a gate length of the gate electrode is greater than twice a thickness of the first compound semiconductor layer, and is equal to or smaller than five times the thickness of the first compound semiconductor layer.

2. The semiconductor device according to Claim 1, wherein the first compound semiconductor layer contains carbon, and a carbon concentration of the first compound semiconductor layer is lower than 1´1017 cm-3.

3. The semiconductor device according to Claim 1 or 2, wherein the gate length of the gate electrode is equal to or shorter than three times the thickness of the first compound semiconductor layer.

4. The semiconductor device according to any one of Claims 1 to 3, wherein the first and second compound semiconductor layers are nitride semiconductor layers.

5. The semiconductor device according to any one of Claims 1 to 4, wherein the first and second compound semiconductor layers contain gallium nitride.

ABSTRACT

Drawings

FIG. 2

GaN(C concentration<1´1017 cm-3)